

REMARKS

Claims 1, 3-17, 19-22, and 24-33 are pending. Claims 1, 3-6, 10-17, 19-22 and 24-33 stand rejected. Claims 7-9 are objected to. Accordingly, claims 1, 3-17, 19-22, and 24-33 are at issue. Further examination or reconsideration is requested.

Claims 1, 12 and 17-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yeh, U.S. Pub. 2004/0059766 in view of prior art disclosed in the application.

Claim 1 recites, inter alia, that the Inverse Fast Fourier Transform circuit has a length of N samples, and is adapted to circularly shift the input data by m samples. Such structure is not shown in Yeh. The Office Action, on page 3, identifies Fig. 8 of Yeh as disclosing a complex rotator. However, that complex rotator does not circularly shift *samples* of data. The complex rotator shown in Figure 8 of Yeh concerns shifting the bits *within* the arithmetic value of a given sample. Additionally, the shifters shown in Figure 8 are also bit-wise shifters, and do not concern shifting entire samples. In short, Figure 8 does not concern shifting samples (as opposed to bits within a sample), and must also therefore fail to disclose shifting samples by “ m ” number of samples.

The circular shift of m *samples*, claimed in claim 1, in contrast, does not involve shifting bits within a sample, but instead concerns shifting entire samples in time relative to a sequence of samples. In summary, the circular shift, as claimed in the present application, changes the time order position of the output samples, whereas the complex rotator of Yeh does not change the time order position of the output samples. Accordingly, Yeh does not disclose the claimed circular shift. Regarding the citation to the prior art example discussed in paragraphs 0036 and 0037, that example does not disclose an IFFT having a length N and a buffer having a length m , where m is less than N , as claim 1 now claims. The known example is disadvantageous because the buffer length is the same as the IFFT length. In the disclosed example, both are length 64, even though the cyclical prefix is only length 16. The present invention, by circularly shifting the time order of the samples within the IFFT, is advantageous because it reduces the required buffer length, preferably to the length of the cyclical prefix.

The combination of Yeh and the prior art example given in the present application fail to disclose two features of claim 1 as noted above and therefore, even if combined, do not render unpatentable the invention now claimed in claim 1. Allowance is respectfully requested.

Claim 12 depends from claim 1 and is patentable over the cited art for the same reasons as claim 1 given above.

Claim 17 claims, inter alia, a means for performing a circularly shifted Inverse Fast Fourier Transform on frequency domain information to generate time domain information, wherein the circular shift is approximately the same as a desired cyclical prefix and input samples for the Inverse Fast Fourier Transform are not multiplied by rotator coefficients. The remarks set forth above with respect to claim 1 are incorporated by reference. In particular, Yeh does not disclose the circular shifting of samples, and therefore cannot disclose a circular shift that is approximately the same as a desired cyclical prefix. Additionally, the example discussed in paragraph 0037 indicates that the buffer would have to be length 64 (the same as the length of the IFFT), and fails to disclose a means for buffering a portion of the time domain signals approximately the same as the desired cyclical prefix, as claimed in claim 17. Thus, the combination of Yeh and the previously known example given in the present application fail to disclose two features of claim 17 and therefore, even if combined, do not render unpatentable the invention now claimed in claim 17. Allowance is respectfully requested.

Claims 19-21 depend from claim 17 and are patentable over the cited art for the same reasons as claim 17 given above. Additionally, with respect to claims 19 and 20, Yeh fails to disclose a means for modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory (claim 19) or a means for modifying the order of the contents of the memory and modifying the control circuit to modify the control of the rotator circuits and butterfly circuits (claim 20), and claims 19 and 20 are patentable for these additional reasons.

Claims 3-6, 10, 11, 13-16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yeh in view of Walton (U.S. Pub. 2004/0081131). Claims 3-6 depend from claim 1, and therefore include all of the limitations of claim 1 and are believed allowable for the same reasons as independent claim 1. The remarks with respect to claim 1 are incorporated herein by reference.

Additionally, claim 4, recites that the Inverse Fast Fourier Transform is adapted to circularly shift the input data by m samples by modifying the memory contents for multiplier circuits with memory and modifying the control for rotator circuits. Claim 5 recites the Inverse Fast Fourier Transform is adapted to circularly shift the input data by m samples by modifying the control for the

first rotator circuit and memory contents of the first multiplier circuit with memory. As set forth above, neither Yeh, Walton, nor the prior art disclosed in the present application teach or suggest modifying an IFFT to circularly shift the data by m samples. Accordingly, neither Yeh, Walton, nor the prior art disclosed in the present application, can teach or suggest the specific ways that the IFFT is modified as recited in claims 4 and 5, i.e., by modifying the memory contents for multiplier circuits with memory and modifying the control for rotator circuits (claim 4) or by modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory (claim 5).

Claim 6 recites another configuration of the IFFT to effect a circular shift of the output of the Inverse Fast Fourier Transform circuit by m samples. In particular, claim 6 recites a control circuit configured to modify the control to the rotator circuit and to selectively control the plurality of butterfly circuits whether the addition operation or the subtraction operation is output first in time. As set forth above, the cited passages of the cited references do not disclose such structure.

Accordingly, claims 4, 5 and 6 are believed allowable for these additional reasons.

Regarding claim 10, as set forth above, Yeh does not disclose the circular shifting of any *samples*, and therefore cannot disclose a control for a first rotator circuit is modified to effect the shift of the samples at the output of the Inverse Fast Fourier Transform by m samples, where m is one fourth of the length of the IFFT. Claim 10 is patentable for this additional reason.

Regarding claim 11, paragraph 0037 of the present application discloses that, in the prior art example, “a buffer of 64 samples is required.” This is the same as the length of the IFFT (see paragraph 0036. In contrast, in claim 11, while the IFFT is 64, the buffer length is only 16. See, claim 1 (“the buffer having length m ”), claim 11 (“the cyclical prefix has a length m equal to 16”). Claim 11 is patentable for the additional reason that the previously known IFFT in paragraph 0037 will not work with a buffer of length 16.

Regarding claim 13, the remarks set forth above with respect to independent claim 1 are incorporated by reference. Claim 13 is patentable over Yeh for the same reasons given with respect to claim 1, and Walton fails to fill the deficiencies in Yeh with respect to the circular shifting of input samples. Additionally, claims 14-16 depend from claim 13, and are allowable for the same reasons as claim 13.

Claims 22 and 24-25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yeh in view of Mazzoni (U.S. Pub. No. 2004/0151110) and admitted prior art. Applicants respectfully traverse the rejection.

Claim 22 claims, inter alia, performing a circularly rotated Inverse Fast Fourier Transform on frequency domain information to generate time domain information without multiplying input samples by rotator coefficients, wherein the amount of the circular shift is the same as the length of the cyclical prefix. The remarks set forth above with respect to claims 1 and 17 are incorporated by reference. In particular, the bit-wise operations in Yeh are not the same as performing a circularly rotated Inverse Fast Fourier Transform, which indicates that the samples are rotated.

Claims 24 and 25 depend from claim 22, and therefore include all of the limitations of claim 22 and are believed allowable for the same reasons as independent claim 22. The remarks with respect to claim 22 as set forth above are incorporated herein by reference.

Claims 26-33 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yeh in view of Walton. Applicants respectfully traverse the rejection.

Claim 26 claims, inter alia, that the output of the transform circuit is circularly shifted by m samples by modifying the control to a first stage rotator circuit and modifying the memory contents of the multiplier circuit. Claim 30 claims, inter alia, that the output of the transform circuit is circularly shifted by m samples by modifying the control to the butterfly circuit, modifying the control to the rotator circuit and re-ordering the memory contents of the multiplier circuit. As set forth above, Yeh and Walton do not teach or suggest this. The remarks set forth above with respect to claims 1 and 17 are incorporated by reference. In particular, the bit-wise operations in Yeh are not the same as circularly shifting entire samples. Neither Walton nor Yeh teach or disclose modifying a transform circuit to achieve a circular shift of samples. Accordingly, claims 26 and 30, and the claims that depend therefrom, are believed allowable over those published applications.


In view of the foregoing remarks, it is respectfully submitted that the present application is now in condition for allowance. Favorable reconsideration and allowance of the present application are respectfully requested.

The Commissioner is hereby authorized to charge any additional fee which may be required for this application under 37 C.F.R. §§ 1.16-1.18, including but not limited to the issue fee, or credit any

overpayment, to Deposit Account No. 23-0920. Should no proper amount be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal, or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 23-0920.

Respectfully submitted,

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July 13, 2009

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